Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. **(Currently Amended)** A method of interconnecting cores in systems-on-chip, said method comprising the steps of:

selecting at least two cores to be interconnected, each core having at least one associated pin classified in terms of predetermined ~~properties~~ functional, structural or electrical characteristics;

automatically assessing the compatibility of at least one pin of at least one core with respect to at least one pin of at least one other core, wherein said assessing comprises performing a compatibility check to determine whether the pins of a given pair of pins are compatible with respect to at least one given ~~property~~ characteristic; and

automatically interconnecting said cores via establishing at least one connection between at least one pair of compatible pins.

2. **(Original)** The method according to Claim 1, further comprising:

automatically assessing, subsequent to said interconnecting step, whether all pins are connected;

if at least two pins are not connected, thereafter applying a protocol to establish at least one additional connection between at least one additional pair of compatible pins.

3. **(Currently Amended)** The method according to Claim 1, further comprising, prior to said selecting step, classifying said cores and said pins in terms of predetermined ~~properties~~ characteristics.

4. **(Currently Amended)** The method according to Claim 3, further comprising, prior to said selecting step, encoding said ~~properties~~ characteristics as binary decision diagram variables.

5. **(Currently Amended)** The method according to Claim 4, wherein said assessing step comprises performing Boolean operations on said binary decision diagram variables to compare and match ~~properties~~ characteristics.

6. **(Cancelled)**

7. **(Currently Amended)** The method according to Claim 3, wherein said assessing step further comprises performing a matching check to determine whether the pins of a given pair of pins exhibit equivalent values associated with at least one given ~~property~~ characteristic.

8. **(Currently Amended)** The method according to Claim 1, further comprising:

subsequent to said interconnecting step, automatically verifying whether the pins in at least one interconnected pair of pins have matching pin ~~properties~~ characteristics.

9. **(Currently Amended)** The method according to Claim 8, further comprising:

prior to said verifying step, establishing a list of pin ~~properties~~ characteristics for which a match between the pins in at least one pair of pins is required;

said verifying step comprising the step of referring to said list of pin ~~properties~~ characteristics to determine whether the pins in at least one interconnected pair of pins have matching pin properties.

10. **(Currently Amended)** A system for interconnecting cores in systems-on-chip, said system comprising:

a selector which selects at least two cores to be interconnected, each core having at least one associated pin classified in terms of predetermined ~~properties~~ functional, structural or electrical characteristics;

an assessing arrangement which automatically assesses the compatibility of at least one pin of at least one core with respect to at least one pin of at least one other core, wherein said assessing arrangement is adapted to perform a compatibility check to determine whether the pins of a given pair of pins are compatible with respect to at least one given ~~property~~ characteristic; and

a connecting arrangement which automatically interconnects said cores via establishing at least one connection between at least one pair of compatible pins.

11. **(Currently Amended)** The system according to Claim 10, further comprising a classifying arrangement which classifies said cores and said pins in terms of predetermined ~~properties~~ characteristics.

12. **(Currently Amended)** The system according to Claim 11, further comprising an encoding arrangement which encodes said ~~properties~~ characteristics as binary decision diagram variables.

13. **(Currently Amended)** The system according to Claim 12, wherein said assessing arrangement is adapted to perform Boolean operations on said binary decision diagram variables to compare and match ~~properties~~ characteristics.

14. **(Cancelled)**

15. **(Currently Amended)** The system according to Claim 11, wherein said assessing arrangement is further adapted to perform a matching check to determine whether the pins of a given pair of pins exhibit equivalent values associated with at least one given ~~property~~ characteristic.

16. **(Currently Amended)** The system according to Claim 10, further comprising a verifying arrangement which verifies, subsequent to interconnecting, whether the pins in at least one interconnected pair of pins have matching pin ~~properties~~ characteristics.

17. **(Currently Amended)** The system according to Claim 16, wherein said verifying arrangement is adapted to refer to a predetermined list of pin ~~properties~~

characteristics to determine whether the pins in at least one interconnected pair of pins have matching pin ~~properties~~ characteristics.

18. **(Currently Amended)** A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for interconnecting cores in systems-on-chip, said method comprising:

selecting at least two cores to be interconnected, each core having at least one associated pin classified in terms of predetermined ~~properties~~ functional, structural or electrical characteristics;

automatically assessing the compatibility of at least one pin of at least one core with respect to at least one pin of at least one other core, wherein said assessing comprises performing a compatibility check to determine whether the pins of a given pair of pins are compatible with respect to at least one given ~~property~~ characteristic; and

automatically interconnecting said cores via establishing at least one connection between at least one pair of compatible pins.